

Combine Boundary Scan with CPU Emulation to Extend Test Coverage



ASSET-InterTech produces boundary scan tools and software. International Test Technologies produce CPU emulation tools, which are optimized for manufacturing test, debug, and repair.

Boundary Scan is a structural test method, whereas CPU emulation is a functional test method. Functional tests, although sometimes difficult to generate, will cover some (usually unknown) structural defects whereas structural tests are unlikely to cover any functional misbehaviors. Discussions between ASSET-InterTech and International Test Technologies showed a potential synergy between the boundary scan and CPU emulation approaches. That is, use boundary scan to structurally test a board, and then use CPU emulation to structurally test those parts not covered by boundary scan, and to implement a basic functional test of the board. ASSET's ScanWorks now includes an emulation function, although in prototype form.

Background

It is assumed that the reader is familiar with boundary scan testing as described in the IEEE 1149.1-2001 boundary-scan Standard.

Emulation testing is used with bus-based boards. The emulator typically replaces some part of the on-board circuitry, and takes control

of the board via one of its buses. Once in control, the emulator can load and run tests and diagnostics on the Unit-Under-Test (UUT).

Emulation was a popular approach in the 80s and early 90s; its decline was driven by the absence of socketed processors and ROMs in new designs, and by increasing processor speeds, which made emulators difficult or impossible to design. However, with the advent of processor debug interfaces, there is now a renaissance of this powerful approach to functional test and diagnosis. A debug interface embeds the traditional emulation functions inside the CPU die, and access to these functions is typically provided through the boundary scan interface. In essence, a 'processor emulator' is now inside the processor!

Typically, the debug functions incorporated include the following:

- Stop the Processor
- Read/Write Memory
- Read/Write I/O
- Breakpoints
- Single Step Code
- Code Trace

Access to the debug functions is typically via the processor's 1149.1 Test Access Port

(TAP), sometimes known as an extended-JTAG (eJTAG) port, plus 2-3 special purpose signals. Processor designers simply extend the 1149.1 instruction set to include vendor-specific instructions for controlling the processor core.

How can the debug interface be used for manufacturing test and diagnosis? The debug interface allows the tester to take control of the processor, and then the processor is simply used as a 'vehicle' for testing the rest of the UUT. For example, the debug interfaces read/write functions can be used to perform memory testing.

Most modern microprocessors and DSPs now include a debug interface.

Example Application

To illustrate the potential synergy between classical structural board test based on boundary scan and emulation functional board test based also on boundary scan using eJTAG ports, we will explore the possibilities on the processor-based board shown in Fig. 1.

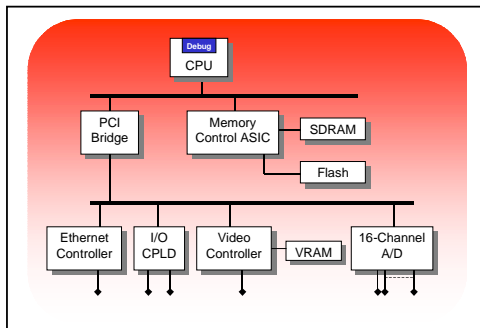


Fig. 1

In Fig. 2, the chips with 1149.1 boundary scan are shown in blue. The board areas covered by boundary scan test are primarily between the boundary-scan devices. Tests are structural only and are generated from CAD data. Diagnostics are to node level. Structural defects associated with the SDRAM and Flash devices can also be tested.

Fig. 3 shows in green the test coverage of CPU emulation. Tests are primarily functional but there will be indirect coverage of

manufacturing defects. Tests are generated manually or semi-automatically, and diagnostics are to functional level.

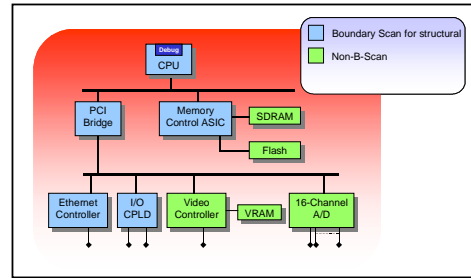


Fig. 2

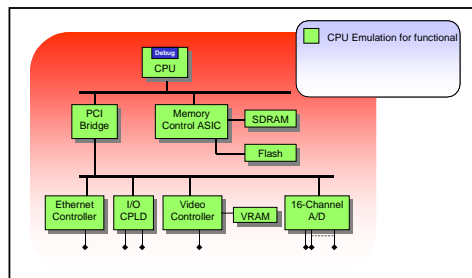


Fig. 3

Although full test coverage is available via CPU emulation, boundary scan can do a better job on certain functions when it is available. This is because test development can be driven from CAD, interconnect pattern generation is fully automatic, and diagnostics usually identify the exact location of opens and shorts. With CPU emulation, test development is a semi-automated process, and diagnostics only identify faulty functions, not nodes.

Fig. 4 shows a combined approach, which optimizes test coverage, test development time, and diagnostic resolution when using both methods.

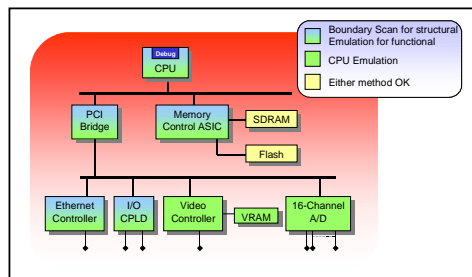


Fig. 4

Considerations and Benefits of a Dual Approach

The same boundary scan pins are used for both test approaches, so switching between structural and functional tests should be seamless.

1. Use boundary scan where possible as vectors and diagnostics can be automatically generated and diagnostics are more specific.
2. Use CPU emulation for testing non-boundary scan parts. Test generation will be semi-automated, and diagnostic resolution will be to functional, not node level.
3. In addition, CPU emulation can provide functional test coverage to both boundary scan and non-boundary scan parts.
4. Memory testing is possible with either method, but only interconnect testing is possible with boundary scan.
5. Analog testing of CPU accessible parts may be possible using CPU emulation.
6. CPU emulation test is at full board speed.
7. CPU emulation can verify loaded software revisions, and check that the board boots under its own software.

Emulation and ScanWorks



ASSET's ScanWorks now has emulator compatibility, and can run test scripts, which have been generated by International Test Technologies CPU emulation equipment.

More Information?

Contact ASSET InterTech or International Test Technologies sales for more information on this innovative combinational test approach.

ASSET InterTech Inc.

Dave Bonnett
Technical Product Manager
dbonnett@asset-intertech.com
972-664-3003
Or contact your local sales representative
<http://www.asset-intertech.com>

International Test Technologies

In US

Tel: (415) 753 5376
Email: sales@intertesttech.com
Web: www.intertesttech.com

In Europe/Asia

Tel: +353-74-9188100
Email: sales@intertesttech.com
Web: www.intertesttech.com

Reference

J Webster et al., "On the synergy of boundary scan and emulation board test: a case study", Digest IEEE Board Test Workshop, 2003, paper 2.3 (Available from contacts above.)

