

JTAG White Paper

JTAG: The Multi-purpose Board Test Interface

JTAG, also known as boundary scan and IEEE 1149.1, is a board-level test interface. Its design and adoption have been driven by diminishing board test access points. Lack of test access has made traditional test approaches, such as ICT, less useful for verifying IC interconnects during manufacturing test.

JTAG Origins

JTAG was originally proposed in the 80's by the Joint Test Action Group (JTAG). This became an official IEEE standard in 1991. It defines a 5-pin interface, a test controller architecture (Test Access Port or TAP), and a mechanism for monitoring and controlling the state of each IC pin during testing. So, the state set by the JTAG sub-system on one IC, can be verified through the JTAG sub-system on another IC. The JTAG interfaces on all ICs are daisy-chained together. Thus, the interconnects between ICs can be verified without the need for test access probes on each IC pin.

Recent JTAG Applications

The primary motivation for JTAG was verifying IC interconnects, which could not be verified using traditional test approaches, such as ICT. However, over the last 15 years, the 5-pin interface has also been used for many other functions. These include:

- Flash Programming
- FPGA/CPLD Programming
- Memory Test
- CPU Emulation
- System-level Test
- BIST Access
- Various Instrumentation Functions

The remainder of this document briefly discusses the above 'non-standard' JTAG applications.

Memory Test

Memory chips do not have a JTAG sub-system, but a memory controller often does. Therefore, the JTAG sub-system on the memory controller can be used to simulate memory read/write cycles. Using these simulations, test patterns can be written to memory, and can then be verified using a simulated read cycle. Memory test algorithms can be constructed using sequences of these read/write cycle simulations.

Flash Programming

As with memory test, read/write cycles simulated via the memory controller, can be used to write to, and thus program flash devices. Flash programming algorithms can be constructed using sequences of these simulated write cycles.

FPGA/CPLD Programming

FPGA and CPLD often require interconnect testing during manufacturing test. The devices also require programming in-situ. Therefore, rather than adding special programming pins, the FPGA/CPLD

vendors use the JTAG pins for device programming. In the past, most device vendors, adopted their own bit-level protocols for programming, but in more recent times a standard has been defined, IEEE 1532, which provides greater JTAG tool and FPGA/CPLD interoperability.

CPU Emulation

As CPUs increased in operation speed, it became impossible to design CPU emulators for software developers. Therefore, the CPU vendors embedded emulation type functions in the CPU (e.g. single step, read/write, etc.), and generally the JTAG port was chosen as the interface port. The bit-level protocols and instructions are often vendor specific, although an attempt has been made at standardization with IEEE 5001 (Nexus).

So, using the CPU JTAG port, it is possible to control the CPU in real time. Essentially, full speed functional test can be carried out via the JTAG port. In essence, JTAG goes beyond just interconnect testing.

For more information see:
http://www.intertesttech.com/download/bscan-cpu_emulation.pdf

System-level Test

Many products contain multiple boards in a backplane. The backplane bus often contains the JTAG interface. These means that if appropriate DFT rules are followed, all JTAG functions can be run across the backplane on each individual board, allowing both full system test and configuration through the 5-pin interface!

BIST Access

Many ICs use Built-in Self Test (BIST) for internal test. Logic and memory BIST are two approaches, which allow an ICs internal circuitry to be verified. Often this can be initiated, and the results returned via the JTAG port.

Intel® IBIST

JTAG interconnect tests are not at normal board operation speed. IBIST, is a new technology from Intel, which is controlled via JTAG. This allows at-speed interconnect testing of high speed differential buses.

Various Instrumentation Functions

The functions presented above are now common uses of the JTAG interface. However, others have been implemented and include:

- SoC Test (IEEE P1500)
- Embedded Instrumentation

Conclusions

For non-intrusive (no test probes) test, the JTAG bus has now become the interface of choice. Progress is continuing with new IEEE initiatives, both for system and IC test. These propose to use the JTAG interface. JTAG is certainly, the way to go!

Links

IEEE Documents:
<http://shop.ieee.org/ieeestore/>

CPU Emulation:
<http://www.intertesttech.com/>