

## Testing and Diagnosing Single Board Computers

The MicroMaster processor board test solutions from International Test Technologies can be used to test all types of CPU-based boards. This application brief shows how the solution can be configured to test a VME or CompactPCI single-board computer based on an Intel Pentium or Motorola/IBM PowerPC microprocessor.

The tester is driven by an external PC, and consists of a CPU emulator, which takes control of the UUT's processor. Once in control, test programs and diagnostics can be directed and sequenced under the control of the host PC. Additionally an I/O emulator is available, which provides the facilities to stimulate and/or measure activity on the board's I/O connector. Using this top-down and bottom-up approach full testing can take place in seconds, rather than minutes

Figure 1 shows the components of the solution, and figure 2 shows an optional fixture, which can be used to automate the connection of UUT to the test instruments – ideal for high volume production test.

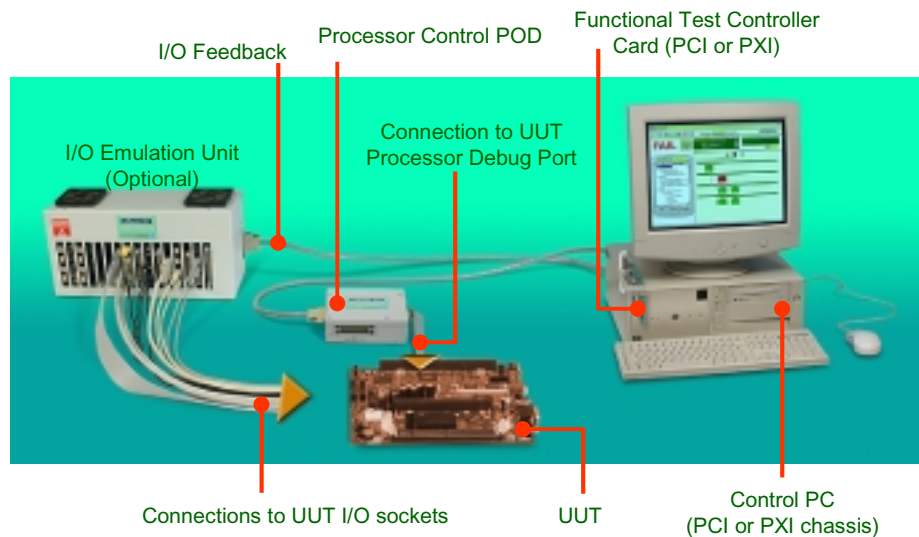


Fig. 1 – Test Solution Components



Fig. 2 – Fixture for Automated Connection

Figure 3 shows how the tester's hardware components are configured for a Single Board Computer application, and the table overleaf shows the test sequence and program, which is run by the tester. Results returned are pass/fail, or pass/fail with full diagnostics to bus and component level.

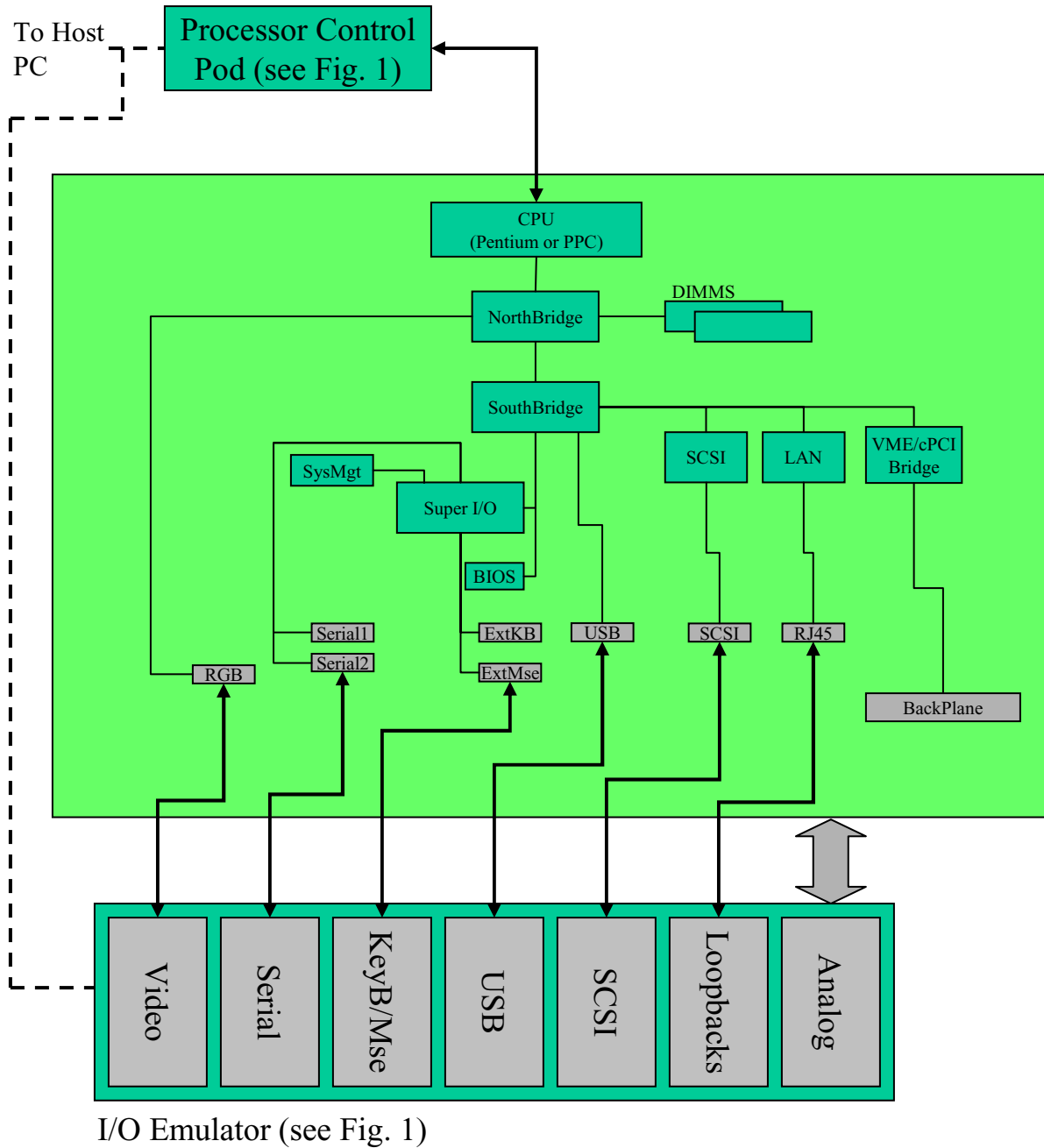


Fig. 3 – SBC Test

## Test Sequence and Coverage

Test Name	Test Sequence	What it Tests
Power	<ol style="list-style-type: none"> <li>1. Power on UUT</li> <li>2. Check key voltages using analog test card.</li> </ol>	<ol style="list-style-type: none"> <li>1. Soft on/off circuitry OK?</li> <li>2. Key voltages within range?</li> </ol>
CPU	<ol style="list-style-type: none"> <li>1. CPU ID Check</li> <li>2. CPU BIST Check</li> <li>3. Take control of CPU</li> </ol>	<ol style="list-style-type: none"> <li>1. JTAG OK?</li> <li>2. CPU OK?</li> <li>3. CPU infrastructure OK?</li> </ol>
General Bus	Boot ROM Bus Test	Verifies all buses from CPU to boot ROM (i.e. host, hub, PCI, LPC, etc.)
NorthBridge	<ol style="list-style-type: none"> <li>1. Register Test</li> <li>2. Configure for normal operation</li> </ol>	<ol style="list-style-type: none"> <li>1. Verifies communications from CPU to NorthBridge.</li> <li>2. Verifies NorthBridge registers.</li> </ol>
SDRAM	<ol style="list-style-type: none"> <li>1. Configure memory</li> <li>2. Memory test for opens, stucks and shorts to all buses</li> </ol>	Verifies all buses and DIMM connectors from NorthBridge to DIMMs.
SouthBridge	<ol style="list-style-type: none"> <li>1. Register Test</li> <li>2. Configure for normal operation</li> <li>3. Legacy functions (timer, DMAC, IntC, CMOS RAM/RTC)</li> </ol>	<ol style="list-style-type: none"> <li>1. Verifies communications and buses from NorthBridge to SouthBridge</li> <li>2. Verifies SouthBridge registers.</li> <li>3. Verifies PC legacy functions.</li> </ol>
USB	<ol style="list-style-type: none"> <li>1. Register Test</li> <li>2. Configure for normal operation</li> <li>3. Data transfers to ITT's USB card.</li> </ol>	<ol style="list-style-type: none"> <li>1. Verifies SouthBridge USB registers.</li> <li>2. Verifies USB device presence.</li> <li>3. Verifies USB channel(s) communication.</li> </ol>
SCSI	<ol style="list-style-type: none"> <li>1. Register Test</li> <li>2. Configure for normal operation</li> <li>3. Loopback test to ITT SCSI loopback card</li> </ol>	<ol style="list-style-type: none"> <li>1. Verifies SCSI controller PCI bus and registers.</li> <li>2. Verifies operation of SCSI bus lines.</li> </ol>

## Test Sequence and Coverage (continued)

Test Name	Test Sequence	What it Tests
LAN	<ol style="list-style-type: none"> <li>1. Register Test</li> <li>2. Configure for normal operation</li> <li>3. Transmit and receive packets at 10M and/or 100M</li> <li>4. Optionally program MACID</li> </ol>	<ol style="list-style-type: none"> <li>1. Verifies LAN controller PCI bus and registers.</li> <li>2. PHY operation</li> <li>3. Verifies connections from PHY to LAN connector.</li> <li>4. Verifies packet transfers to/from LAN.</li> </ol>
Super I/O	<ol style="list-style-type: none"> <li>1. ID Check</li> <li>2. Register Test</li> <li>3. Configure for normal operation</li> </ol>	<ol style="list-style-type: none"> <li>1. Verifies communications from CPU to SIO.</li> <li>2. Verifies SIO registers.</li> </ol>
System Management Controller (SysMgt)	<ol style="list-style-type: none"> <li>1. EEPROM ID</li> <li>2. Temperature Sensor Check</li> </ol>	<ol style="list-style-type: none"> <li>1. Access to configuration eeprom.</li> <li>2. Operation of temperature sensor.</li> </ol>
Serial	<ol style="list-style-type: none"> <li>1. Register Test</li> <li>2. Loopback test of tx/rx and control lines.</li> </ol>	<ol style="list-style-type: none"> <li>1. Verifies serial controller registers.</li> <li>2. Verifies tx/rx and control lines from controller to serial port connector(s).</li> </ol>
Ext Keyboard	<ol style="list-style-type: none"> <li>1. Register and self test to keyboard controller.</li> <li>2. Generate keypress(es) using ITT keyboard/mouse card and verify keycode at keyboard controller.</li> </ol>	<ol style="list-style-type: none"> <li>1. Verifies keyboard controller access from CPU.</li> <li>2. Verifies keyboard port.</li> </ol>
Ext Mouse	<ol style="list-style-type: none"> <li>1. Register test.</li> <li>2. Generate mouse click(s) using ITT keyboard/mouse card and verify returned codes at controller.</li> </ol>	<ol style="list-style-type: none"> <li>1. Verifies mouse controller access from CPU.</li> <li>2. Verifies mouse port.</li> </ol>
BIOS ROM	<ol style="list-style-type: none"> <li>1. ID Check</li> <li>2. CRC Check</li> </ol>	<ol style="list-style-type: none"> <li>1. Verifies access to boot ROM from CPU.</li> <li>2. Verifies boot ROM contents.</li> </ol>

## Test Sequence and Coverage (continued)

Test Name	Test Sequence	What it Tests
Video	<ol style="list-style-type: none"><li>1. Run BIOS</li><li>2. Initialise selected video mode(s) and verify using ITT RGB check card or operator.</li></ol>	<ol style="list-style-type: none"><li>1. Verifies BIOS boot.</li><li>2. Verifies access from CPU to video controller.</li><li>3. Verifies RGB and/or LCD ports.</li></ol>
PCI to VME/cPCI Bridge	<ol style="list-style-type: none"><li>1. Register test to bridge</li><li>2. Configure bridge for normal operation.</li><li>3. Bi-directional transfers to remote card.</li></ol>	<ol style="list-style-type: none"><li>1. CPU can communicate with bridge.</li><li>2. Bridge registers.</li><li>3. Operation of bridge.</li><li>4. Operation of backplane.</li></ol>

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